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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/875,202	06/07/2001	John Gordon Hogeboom	85773-40D	8101

28291 7590 09/12/2005

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EXAMINER	
DUONG, FRANK	
ART UNIT	**PAPER NUMBER**
2666	

DATE MAILED: 09/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/875,202	HOGEBOOM, JOHN GORDON	
	Examiner	Art Unit	
	Frank Duong	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15,17 and 22-27* is/are rejected.

7)☒ Claim(s) *16 and 18-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is a response to the Preliminary Amendment (PA) dated 06/07/01. The PA requested to cancel claims 1-14 from the application and add claims 16-28 to the application. It appears that claim 15 is missing.

2. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 16-28 have been renumbered 15-27, respectively.Thus, renumbered claims 15-27 are pending in the application.

Information Disclosure Statement

3. The information disclosure statement filed 09/12/01 complies with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609. It has been considered and placed in the application file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 15, 17 and 22-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Ferraiolo et al (USP 5,568,526) (hereinafter "Ferraiolo").

Regarding **claim 15**, in accordance with Ferraiolo reference entirety, Ferraiolo discloses a data communication system (Fig. 1), comprising:

a) a first input for receiving data, said data being characterized by a bit time (*Fig. 1; input from SIDE A LOGIC into CHIP A*);

b) a second input for receiving data control information (*Fig. 1; 33 or col. 3, lines 28-33; links acknowledgement signals and link reject signals*);

c) an encoder unit (*Fig. 1; 24*) coupled to said first and second inputs (see Fig. 1 for connection), said encoder unit operative to:

i) generate clock information (Fig. 2; TRANSMIT CLOCK 27);

ii) process said clock information and said data control information for generating a clock and control signal, said clock and control signal having high and low times in units equal to one said bit time (*col. 4, lines 1-19*);

d) at least one data channel *(Fig. 1; 16 and col. 3, lines 11-12)*; and

e) a clocking and control channel *(Fig. 1; 16 and col. 3, lines 12-13)*, said encoder unit (*Fig. 1; 24*) operative to transmit said data over said at least one data channel and to transmit said clock and control signal over said clocking and control channel (*col. 3, lines 11-13 and col. 4, lines 13-19*).

Regarding **claim 17**, in addition to features recited in base claim 15 (see rationales discussed above), Ferraiolo further discloses wherein said clocking and control channel (*Fig. 1; 16 and col. 3, line 12* or *Fig. 2; DIFFERENTIAL SIGNALS*) is

characterized by a clock rate and said at least one data channel carries data multiplexed at a multiplexing cycle rate, said clock race being substantially equal to said multiplexing cycle rate (*col. 4, lines 13-19 or line 56*).

Regarding **claim 22**, in addition to features recited in base claim 15 (see rationales discussed above), Ferraiolo further discloses a) a decoder unit for receiving data and the clock and control signal over said data channel and said clocking and control channel, respectively, said decoder unit operative to: i) extract from said clock and control signal said clock information and said data control information; process said data on a basis of said clock information and said data control information for generating a data signal; an output for releasing said data signal to a data processing device (*note: the claim calls for elements at a receiver side corresponding to elements in Chip B of Fig. 1*).

Regarding **claim 23**, in addition to features recited in base claim 22 (see rationales discussed above), Ferraiolo further discloses wherein said data channel is selected from the group consisting of a cable, an optical fiber and an air interface (*col. 1, line 49 and thereinafter*).

Regarding **claim 24**, in addition to features recited in base claim 22 (see rationales discussed above), Ferraiolo further discloses wherein said clocking and control channel is selected from the group consisting a cable, an optical fiber and an air interface (*col. 1, line 49 and thereinafter*).

Regarding **claim 25**, in accordance with Ferraiolo reference entirety, Ferraiolo discloses an encoder (Fig. 1; 18 and 24) for use in a data communication system (Fig.

1), said encoder connected at least one data channel and a clocking and control channel (*col. 3, lines 11-12*), said encoder comprising:

a) a first input for receiving data, said data being characterized by a bit time (*Fig. 1; input from SIDE A LOGIC into CHIP A*);

b) a second input for receiving data control information (*Fig. 1; 33 or col. 3, lines 28-33; links acknowledgement signals and link reject signals*);

c) a processing unit (Fig. 1; 24) operative to: i) generate clock information (Fig. 2; 27) ii) process said clock information and said data control information for generating a clock and control signal, said clock and control signal having high and log times in units equal to one said bit time (*col. 4, lines 1-19*);

d) a first output for transmitting said data over the at least one data channel *(Fig. 1; 16 and col. 3, lines 11-12)*;

e) a second output for transmitting said clock and control signal over the clocking and control channel *(Fig. 1; 16 and col. 3, lines 12-13)* (*col. 3, lines 11-13 and col. 4, lines 13-19*).

Regarding **claim 26**, the claim calls for a decoder having the elements mirrored elements in the encoder of claim 25. Thus, it is rejected by the same rationales discussed above.

Regarding **claim 27**, in accordance with Ferraiolo reference entirety, Ferraiolo discloses a data communication system (Fig. 1), comprising:

a) a first input means for receiving data, said data being characterized by a bit time (*Fig. 1; input from SIDE A LOGIC into CHIP A*);

b) a second input means for receiving data control information (*Fig. 1; 33 or col. 3, lines 28-33; links acknowledgement signals and link reject signals*);

c) encoder means (*Fig. 1; 24*) coupled to said first and second input means (see Fig. 1 for connection), said encoder means operative to:

i) generate clock information (Fig. 2; TRANSMIT CLOCK 27);

ii) process said clock information and said data control information for generating a clock and control signal, said clock and control signal having high and low times in units equal to one said bit time (*col. 4, lines 1-19*);

d) at least one data channel *(Fig. 1; 16 and col. 3, lines 11-12)*; and

e) a clocking and control channel *(Fig. 1; 16 and col. 3, lines 12-13)*, said encoder means (*Fig. 1; 24*) operative to transmit said data over said at least one data channel and to transmit said clock and control signal over said clocking and control channel (*col. 3, lines 11-13 and col. 4, lines 13-19*).

Allowable Subject Matter

5. Claims 16, 18-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record, considered individually or in combination, fails to fairly show or suggest the claimed invention of base claim 15 and further limit with a novel and unobvious limitation of "*wherein said clock and control signal is characterized by*

first and second edges, said first edge having fixed phase and said second edge being phase-modulated", structurally and functionally interconnected with other limitations in the manner as recited in the dependent claims 16 and 18-21.

Conclusion

6. The prior art made of record and not relied upon at this time is considered pertinent to applicant's disclosure. Examiner reserves the right to use these references in the subsequent Office Action should a respond to this Office Action overcome this applied art.

Capowski et al (USP 5,513,377).

Halma et al (USP 5,522,088).

Gregg et al (USP 5,651,033).

Greg et al (USP 5,598,442).

Self et al (USP 5,623,644).

Self et al (USP 5,634,043).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frank Duong whose telephone number is 571-272-3164. The examiner can normally be reached on 7:00AM-3:30PM, Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

FRANK DUONG
PRIMARY EXAMINER

September 8, 2005